ABSTRACT

A pipelined microprocessor for processing instructions includes at least one pipeline. The pipeline includes and instruction fetching functional stage, an instruction decoding functional stage, an execution functional stage comprising a number of execution units and a commit functional stage. The commit functional stage includes or is associated with a reorder buffer. Detecting means are provided for detecting instruction irregularities. When an instruction irregularity is detected, an irregularity indication and a flush instruction are generated. The irregularity indication is used to initiate a flush made whereas the flush instruction, when received in a stage or unit set in flush mode, resets the flush mode in said stage/unit.